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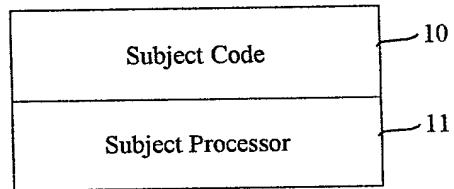


Fig. 1

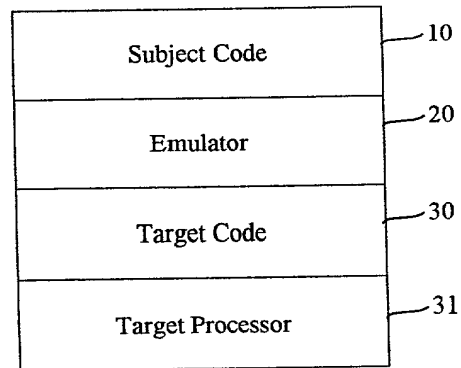


Fig. 2

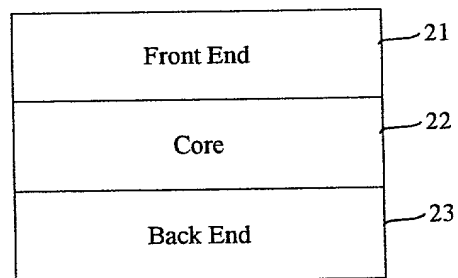


Fig. 3

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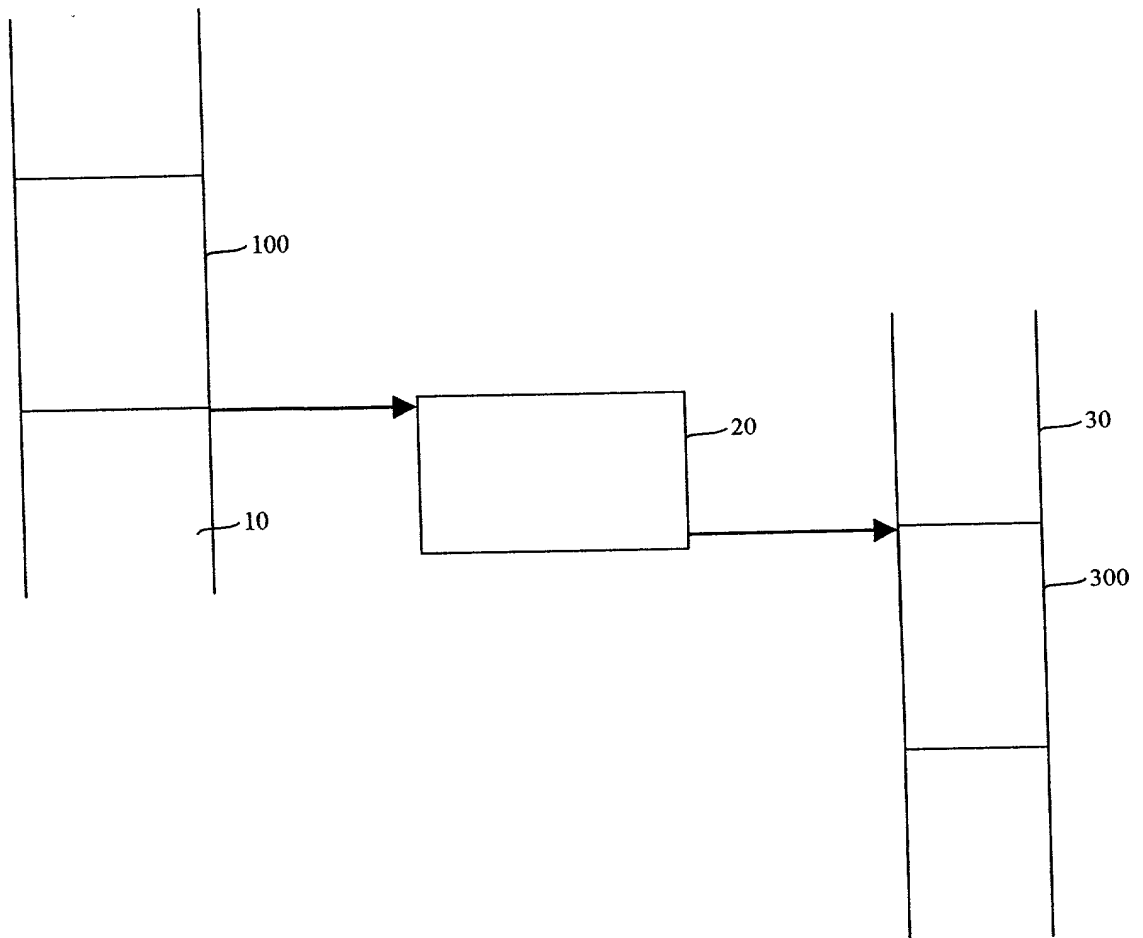


Fig. 4

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Register Memory Map

Register	Target Set A Values	Target Set B Values
Reg X	Reg X _A Definitive	Reg X _B Speculative
Reg Y	Reg Y _A Definitive	Reg Y _B Speculative
...

Fig. 5

Register Memory Map

Register	Target Set A Values	Target Set B Values
Reg X	Reg X _A Definitive	Reg X _B Speculative
Reg Y	Reg Y _A Speculative	Reg Y _B Definitive
...

Fig. 6